Silicon photonics technology: past, present and future

Richard Soref

Air Force Research Laboratory, Sensors Directorate, AFRL/SNHC, Hanscom AFB, MA 01731

ABSTRACT

Due to recent investments by government and industry, silicon-based photonics has a chance of becoming “the” mainstream photonics technology. This paper presents a survey of recent results found in journal articles and conference proceedings. Emerging trends in silicon-based photonic components (waveguides, ultrafast modulators, switches, light sources, detectors, direct bandgap SiGeSn/GeSn devices, photonic-crystal and plasmonic devices) are identified and discussed. In principle, Si PICs and OEICs can operate anywhere within the 0.3 to 100 µm wavelength range—enabling transceivers, on-chip processing, and interfacing with fibers or free-space light beams. Thus, in addition to the very important 1.55 µm telecomm applications, there are significant Si photonic opportunities throughout the infrared-and-visible spectrum. The push towards smarter, ever-denser on-chip photonic networks, drives a “convergence” of micro-, nano- and plasmo- photonic techniques for progressively smaller devices (Moore’s law for photonics) and for improved functionality of modulators, switches, emitters, detectors, waveguides, resonators, tapers and filters. This convergence includes composite components: monolithic integration of microstrip waveguides, 2D and 3D photonic-crystal elements and metal/Si plasmon-optics that utilize buried or surface-mounted 2D arrays of metal stripes or nanodots.

Keywords: Silicon, waveguides, optoelectronics, SiGe, infrared, THz, lasers, modulators, photonic crystal, plasmons

INTRODUCTION

Other authors in this Photonics West Conference 5730 will cover in detail the topics of optoelectronic integration, CMOS compatibility, optical MEMs, sensor applications, optical receivers, optical interconnect techniques, and nonlinear Raman effects. Rather than expounding upon these topics, I shall survey recent developments in silicon-based photonic components including lasers, light emitters, and waveguided components such as ultrafast electrooptic modulators. Results taken from the literature and conference proceedings are presented in this paper. The paper focuses upon photonic structures that are amenable to Si-based optoelectronic integration. A goal of this paper to identify science-and-technology trends that are emerging in photonic device construction, in device-related Group IV materials science, and in “new” wavelength ranges available for photonic circuit operation—wavelength bands currently less exploited than the 1550 nm telecomm regime. The significant investments in Si-based optoelectronics made by AFOSR, DARPA and Intel Corporation during the year 2004—fundings discussed elsewhere in this conference—are likely to accelerate the growth of this field. That is why 2004 marks a turning point in the history of silicon photonics.

1. WAVELENGTH RANGES OF OPERATION

Today, the telecomm/datacomm applications at 1.5-1.6 µm are the principal “drivers” of silicon photonics (1.55 µm is also an eye-safe wavelength for military applications), however it is worth considering applications at other wavelength regions because those uses could become economically significant. The wavelength range over which a Si-based photonic integrated circuit (PIC) or optoelectronic integrated circuit (OEIC) can operate depends upon whether the photonic waveguide material is silicon or another material. Intrinsic silicon is transparent from its 1.1 µm indirect bandgap wavelength out to about 100 µm, allowing a wide scope for silicon waveguide operation. Moreover, if the core layer of the silicon waveguide is very thin (several nanometers) and is quantum confined, then the Si bandgap widens and the Si transparency extends to shorter wavelengths, 800 nm or less, enabling visible and near-infrared waveguide
transmission\(^1\). In situations where the optical signal beams are incident normally from free space upon the OEIC chip, as in the optical interconnect arrangement, the chip will work over 450 to 850-nm if the chip contains Si photodetectors and Si CMOS light emitters\(^2\). A waveguided version of this OEIC will be feasible if the waveguide cores are silicon nitride\(^3\).

Over the past decade, it has become clear that individual Si or SiGe/Si components will function well at the mid-wave, long-wave and very long-wave infrared (THz) ranges. Examples of electroluminescent emitters are the SiGe/Si quantum-cascade emitters that have been developed for 30 to 100 \(\mu\)m on two DARPA-funded Air Force contracts\(^4,5\) (monitored by this author), and the 8 to 14 \(\mu\)m SiGe/Si quantum-cascade emitters demonstrated on the European Union SHINE project. These cryogenically cooled QC emitters are pre-cursors of quantum cascade lasers, which, it is hoped, will be developed within a year or two. These longwave and THz emitting diodes are grown strain-balanced upon an SiGe buffer upon silicon. Another important group of Terahertz emitting diodes are the impurity-based LEDs such as cryo-cooled Si:B, Si:P, Si:Ga [see the publications of Prof. James Kolodzey at www.ee.udel.edu/~kolodzey/publications/iskpubsjun04.html]. These devices require no epitaxy, are fairly efficient and simple in construction. Researchers in Russia have also reported strong THz emission from cryo-cooled resonant-state-impurity emitters in strained silicon or SiGe, where the strain in the crystal is analogous to the static magnetic field applied within the electrically and magnetically biased p-type Germanium THz laser-- a 4K laser that uses an LH to HH transition\(^6,7\).

Progress on Si-based photodetectors has also been made throughout the infrared spectrum; sensors including Schottky-barrier photodetectors for the NIR, hetero-internal photoemission (HIP) p-SiGe/Si multi-quantum well artificial Schottky-barrier diodes for 3 to 5 \(\mu\)m and 8 to 12 \(\mu\)m sensing\(^8\), cryo-cooled SiGe/Si p-doped quantum well infrared photodetectors (QWIPs) for the entire range from 6 \(\mu\)m out to 50 \(\mu\)m (the latter wavelength attained recently\(^9,10,11\)), with the wavelength of peak response being governed by quantum-well depth which in turn depends upon alloy composition. Integrated MOSFET readout of an 8 to 12 \(\mu\)m SiGe/Si QWIP has been proven in a Si-OEIC\(^12\). Work has been done on normal incidence p-Ge/SiGe QWIP structures for 2 to 3 \(\mu\)m. They are multi quantum well structures grown strain-balanced on an SiGe buffer\(^13,14\). All of the aforementioned QWIPs are laboratory demonstrations. A worthy challenge for the future is to develop those QWIPs into practical devices—both as focal-plane imaging arrays and as point sensors. Room-temperature silicon micro-bolometers, usually deployed in N x N pixel imaging arrays, can sense over a wide infrared spectrum including Terahertz. Strides have also been made in extrinsic silicon photconductor consisting of cryo-cooled crystal-silicon diodes doped with shallow donor or acceptor impurities\(^15\). Impurity photoconduction has been observed from 10 \(\mu\)m out to 50 \(\mu\)m (recently, by Prof. Kolodzey). Blocked impurity-band (BIB) detectors out to 40 \(\mu\)m have were realized in Si:Sb and Si:As\(^16\).

These LED, laser and PD components generally require cooling within the 4K to 77K liquid-helium to liquid-nitrogen range, and the amount of cooling needed increases with increasing infrared wavelength. I believe that Si PICs and OEICs are generally feasible throughout the entire infrared range, with the proviso that the OEIC transistors will have to “endure” whatever cooling is imposed upon the optical circuit. (This PIC feasibility has not yet been tested at longer waves.) I shall also predict that OEIC fiber-optic systems (chips linked to fibers) will become feasible over the wide infrared spectrum. One reason for saying this is that single-mode fibers are already available for transmission within the 1 \(\mu\)m to 18 \(\mu\)m spectrum, and for 100 to 300 \(\mu\)m. To supplement the well-known glass fibers (\(\lambda < 2 \mu\m\)), we now have chalcogenide IR-glass fiber (CIR) for 2 to 6 \(\mu\m\) and polycrystalline AgCl:AgBr infrared fibers (PIR) for 4 to 18 \(\mu\m\) (both from ART-Photonics\(^17\)). Due to the LWIR transparency of Teflon, I speculate that malleable materials related to Teflon may allow creation of fiber optics for 30 to 100 \(\mu\m\) wavelengths. It has already been proven that fiber-optics for wavelengths of 100 to 300 \(\mu\m\) are possible using plastic photonic-crystal fibers made from tubes and filaments of high-density polyethylene\(^18\). The PhC-fiber approach will probably apply from 18 to 100 \(\mu\m\).

A strategy that I suggest for MWIR/LWIR optoelectronic system is to separate the cooled and uncooled portions. I propose uncooled, room-temperature functioning for the active, LWIR electrooptical PIC (the OE chip without sources and detectors) that couples to free-space light beams or to infrared fibers. In this scenario, off-chip “remote” IR transmitters and receivers would send IR signals to and from the uncooled EO PIC chip via short lengths of IR fiber. Those sources and sensors could reside upon a second, cooled chip. With these ideas in mind, I propose silicon integrated photonics at midwave and longwave IR, a new paradigm. The practical issues are whether low-loss
waveguides-on-Si and fiber-optics are available at the particular wavelengths of interest. I expect SOI waveguides will be quite viable at mid-infrared due to the high transmission of the buried silicon-dioxide layer (BOX). To be specific, fused silica transmits well from 0.25 \(\mu\)m to 2.6 \(\mu\)m and from 3.0 \(\mu\)m to 5.4 \(\mu\)m. [Silicon-on-sapphire transmits from 0.2 to 6.0 \(\mu\)m.] Although SiO\(_2\) has a “relative transparency” window from 10 to 11 \(\mu\)m (Fig. 9 of [19]), the absorption coefficient is still quite high (Fig. 8 of [19]), thus SOI guides at the popular 10.6 \(\mu\)m wavelength will suffer from high attenuation due to loss in the lower cladding. However, as has been demonstrated by Vlasov’s group at IBM, this problem can be solved by undercutting the SOI locally, that is, by etching away the BOX locally beneath the waveguide’s area via buffered oxide etching (BOE), leaving a locally suspended silicon membrane clad above and below by air\(^{20}\)—as is also done in photonic-crystal integrated circuits at the University of Delaware and elsewhere. Vlasov implies that the Si membrane process is compatible with a commercial CMOS Fab. In addition, it is clear that low-loss SiGe/Si waveguides can be made for 10.6 \(\mu\)m operation. Thus, I shall briefly propose and examine 10.6 \(\mu\)m PICs. The reasons why a \(\sim\)10 \(\mu\)m PIC should be built and tested are: (1) the PIC would demonstrate component integration and on-chip IR signal processing, (2) lithographic tolerances are greater for these “larger” components, (3) the PIC can couple to free space inputs and outputs, (4) the PICs enable sensing and other applications within the 8-12 \(\mu\)m atmospheric transmission window, (5) the free carrier plasma dispersion effect for modulation and switching is 47 times larger at 10600 nm than it is at 1550 nm, (6) photonic networks developed at 10 \(\mu\)m can be scaled readily to longer wavelengths such as 50 \(\mu\)m, (7) single-mode fibers at 10 \(\mu\)m are available now.

2. DIRECT BANDGAP GROUP-IV HETEROSTRUCTURES

The “Atwater Group” at CalTech led by Prof. Harry A. Atwater has been a leader in developing direct-gap GeSn alloys-on-Ge. They also reported self-assembled Sn nanodots (with a \(\sim\)0.4 eV bandgap) in a silicon matrix. Their important and pioneering efforts are summarized on [http://deadalus.caltech.edu/publications.html](http://deadalus.caltech.edu/publications.html), and their recent work on plasmon optics is very strong. During the past five years, cutting-edge research on GeSn has been done by scientists at Arizona State University and ASU is now emerging as a major force in this area.\(^{21-28}\) Professor John Kouvetakis’ group has emerged as a leader in this field, and the theory work of Prof. Jose Menendez has become essential in understanding the band offsets in the heterostructures as well as the alloy bandstructure. Prof. Kouvetakis ([http://www.public.asu.edu/%7Ekouvetak/publications.htm](http://www.public.asu.edu/%7Ekouvetak/publications.htm)) has developed low-temperature CVD growth of GeSn and SiGeSn using unique chemical precursors developed at ASU. An SiGeSn buffer can be grown directly on Si, and the top surface of the virtual substrate has very few defects. In layered structures, alternation of Ge with GeSn, or GeSn with SiGeSn is quite feasible. Thus simple heterostructures or multiple-quantum-well structures can be produced. With these MQWs, variety of new LWIR intersubband devices (lasers, sensors, etc) can be made. Several years ago, I suggested\(^{29}\) that tensile-strained Ge will have a direct bandgap when grown upon GeSn, but recent ASU work shows that the SiGeSn template\(^{30}\) rather than GeSn will give the direct-gap Ge. In addition, ASU has found that Type I band alignment is available for direct-bandgap QWs in their Sn-containing group IV heterostructures. This implies that direct band-to-band photodetectors, modulators, and light-emitting diodes (even lasers) should be feasible in these group IV systems, as described in an invention disclosure\(^{31,32}\). The QW material, Ge or GeSn, for example, is equivalent in its effect to that of a III-V semiconductor like InAs. At this time it is not entirely clear whether SiGeSn is compatible with a commercial CMOS process. If it is, that would open the door to on-chip direct-bandgap band-to-band devices.

A few years ago, the indirect gap alloy SiGeC (with substitutional C up to 2%) was investigated and waveguiding in SiGeC/Si was demonstrated. Less is known about the SiC, the SiSn and SiSnC alloys. It is fascinating that, in theory, the compounds CSi\(_2\)Sn\(_2\) and CGe\(_2\)Sn lattice-match crystal Si within 0.5 to 1\%\(^{33}\).

3. LIGHT EMITTERS AND LASER CANDIDATES

Progress has been made on many fronts in silicon-based light emitters and laser candidates. This topic is “voluminous.” Here, I shall survey a few of the recent developments, focusing upon unusual and exotic approaches. The selection of topics here is rather arbitrary and the coverage of light emitting techniques is not complete. With this caveat, I shall begin with the room-temperature silicon Raman laser, developed in Dr. Bahram Jalali’s group at UCLA\(^{34}\). This is probably the most significant light-source development of 2004, although the Raman laser is optically pumped by another laser, rather than being electrically injected. This device, which can in principle be implemented in an all-silicon resonator, has good potential for mid-IR operation, and the laser generally extends the wavelength range of the pumping

Proc. of SPIE Vol. 5730  21
source. Erbium ions form the basis of important 1.55 µm emitter techniques. With sponsorship from DARPA, a contractor will investigate a solid-state 1.55 µm emitter that contains as many as $10^{22}$ Er ions per cubic centimeter. Professor Jimmy Xu at Brown University has reported laser-like emission at 1.3 µm from a periodic all-silicon nanostructure formed on SOI using an hcp self-organized array of nanopores. Under optical pumping at $T < 70$K, he found classical lasing characteristics. This device has potential for 300K operation as well as electrical injection. Professor Chen Tsai at UC Irvine has observed 1.21 µm stimulated emission at room temperature from an all-silicon pn junction diode that has “nano structuring” in the p-region of the ridge waveguide. I believe that this electrically pumped emission could be shifted to the 1.55 µm regime by employing a nanostructured SiGe diode whose indirect bandgap is at 1.5 µm. For FY05, AFOSR is soliciting Phase-I proposals on a new and important topic, STTR topic AF05-T013, “Silicon-based Lasers for All-Optical Integrated Systems.” Concerning quantum effects, it is intriguing to see how the luminescence of crystal silicon shifts towards the blue when the Si layer is quantum confined. The photoluminescence experiments of Cho et al. on an ultrathin c-Si layer between $a$-SiO$_2$ and c-SiO$_2$ reveal a peak emission at 770 nm in a 1.4 nm Si layer cooled to 10K. The peak shifted consistently as the layer was thinned from 2.4 nm to 0.8 nm. Dr. Martin Green has proposed electrical PIN excitation of such a waveguided QW Si layer.

### 4. SILICON-BASED WAVEGUIDE STRUCTURES

Some of the earliest waveguides were defined by impurity doping in bulk silicon, n$^+$ on n, or p$^+$ on p structures. These have become overshadowed by silicon-on-insulator (SOI) waveguides, the dominant type today. SOI will probably be the prime waveguiding technique by 2010 for two important reasons: SOI is definitely CMOS compatible, and the semiconductor roadmap shows that fully depleted SOI CMOS will be the most important silicon electronics technology of the future. What are the general criteria for a practical waveguide on silicon? Janz and co-workers have given a good synopsis. They say the most-needed features are: low propagation loss, ease-and-versatility of coupling fiber- or free-space-beams into and out of the waveguide, control of the optical mode polarization, and compatibility of the waveguide’s fabrication process with industrial CMOS processing. The loss is determined mainly by the sidewall roughness and by the transparency (intrinsic loss) of the core. Wall smoothing is being developed, and good solutions to the fiber coupling problem have been found in the form of 3D silicon waveguide tapers, either a horn initially wider than the strip or a Si strip that tapers down to a narrow point. Janz’ group at NRC Ottawa has explored graded-index tapers. TE/TM polarization control is usually needed for optical routing switches, and in some PICs polarization-independent waveguides are required. The polarization issues have not been fully resolved.

The list of Si-based waveguide structures that have been proven experimentally is rather long and grows each year. Here is an attempt to present a complete list of present-day waveguides, constructed mainly in the shape of ridges (ribs), strips (photonic wires), rings, or disks: n$^+$/n Si, p$^+$/p Si, silica (with a doped core) upon silicon$^{41}$, SOI$^{52}$, silicon oxynitride on SiO$_2$ on Si, Si$_3$N$_4$ on SiO$_2$ on Si, nanocrystalline Si within SiO$_2$ on Si, polycrystalline Si on Si, nanocrystalline Si in SiO$_2$ on Si, β-SiC on SiO$_2$ on Si (SiCOI and SICOI), silicon on sapphire, low porosity porous-Si upon high-porosity porous-Si, amorphous hydrogenated Si on Si, anti-reflecting resonant optical waveguides (ARROW) upon Si, amorphous hydrogenated SiC on ZnO on Si, low-index core (SiO$_2$ or air) “hollow” guides with photonic-crystal cladding, double SOI (Si/SiO$_2$/Si), SiGe upon Si, SiGeC upon Si, a-SiC:H/a-Si:H/Si, silicon line-defect in a Si-membrane photonic-bandgap lattice, self-collimated waveguide in a dispersion-engineered Si-membrane photonic crystal, electrooptic waveguide on low density polymer on Si, BaTiO$_3$ on MgO on Si, LiNbO$_3$ epitaxy on Si, metal-dot plasmonic array on Si, silicon upon a buried layer of silicide (CoSi$_2$ or NiSi$_2$) on silicon, SiGe/Si surface-plasmon waveguide gold-coated on top and bottom, SiGe/Si multi quantum well stack grown strain balanced upon an SiGe buffer on Si, deep, nanometer-diameter holes in a dielectric that are coated on the inside with Si or Ge.

Looking to the future, here is a list of waveguide types that I expect to be built and tested within the next few years: (1) layered heterostructures such as GeSn/Ge/SiGeSn on Si, or SiGeSn/GeSn/SiGeSn on Si, which can be asymmetrically strained or (preferably) coherently strained strain-balanced alloy-heterostructure waveguides wherein the waveguide core alloy has a higher index than that of the buffer-on-Si or of the Si substrate, (2) a layered multi-quantum well (MQW) alloy heterostructure of GeSn/Ge on SiGe/Si or SiGeSn/GeSn on SiGeSn/Si, (3) quantum-confined SOI having a top Si layer less than 10 nm thick, (4) plasmonic waveguides with a metal dot or metal strip array buried beneath the surface of an Si wafer, (4) tensile-strained-silicon-on-insulator (s-SOI), (5) silicon-germanium-on-insulator (SGOI), (6) germanium-on-insulator (GOI), (7) silicon-on-epitaxial-insulator (SOEI) such as crystal CeO$_2$ or HfO$_2$. 

---

22 Proc. of SPIE Vol. 5730
grown epitaxially upon a silicon wafer with a layer of c-Si then grown upon the oxide layer, (8) N-layer SOI offering N independent Si levels for guided light transmission together with “optical vias” for vertical interlevel optical communication, (9) a 3-dimensional Si photonic crystal offering sub-surface self-collimated waveguides and interlevel communications within a 3-dimensional silicon photonic crystal.

5. SWITCHES AND ULTRAFAST ELECTROOPTICAL MODULATORS

The multi-Gigabit/s speeds required for 1.55 µm modulators in future SiOE chips could surely be met by Pockels- or Kerr-effect (field-effect) electrooptic devices made of polymer-on-silicon, for example, or of BaTiO3/MgO/Si. However, the CMOS compatibility requirement might impose a “semiconductor approach” -- the constraint that the core and/or cladding of the waveguided modulator be made out of some combination of Si, SiO2 and SiGe. Paper 5730-14 at this conference suggests that EO polymer devices are CMOS integratable, which will be proven during the next few years. However, if the modulator core is “semiconductor constrained,” then it appears that the physical mechanism for the modulator will have to be either the free-carrier plasma (FCP) effect or the Franz-Keldysh effect (FKE). The free carrier plasma device would employ injection or depletion or accumulation of carriers, and it may require ion implantation in the core to reduce the minority carrier lifetime well into the picosecond range. Industry, most notably Intel, has lead the way into the GHz domain with a 1 Gb/s MOS accumulation modulator device43 (2.5 mm-long phase shifters within a longer MZI), and their modeling shows extension to 10 GHz, conservatively. Now government, notably the DARPA EPIC program, is sponsoring the semiconductor approach (to great effect, I think). Consequently, I estimate that 20 Gb/s will be achieved experimentally by 2007. Prospects also look quite good, in my opinion, for demonstrating 40 Gb/s and even 100 Gb/s by the year 2010. I did not anticipate this when first investigating modulation via free carriers. Regarding the Franz-Keldysh effect, this effect peaks at a wavelength corresponding to the indirect bandgap of the core material, which is approximately 1.1 µm for Si. Thus, for a 1.55 µm FKE modulator, the waveguide core should be Si1-xGex with x chosen for optimum ∆n/∆E. The assumption here is that SiGe waveguides upon silicon would be quite compatible with SiOE integration, as well as SOI guiding, and this seems a valid assumption to me.

For routing of infrared signals on the SiOE chip, such as 1 x N and M x N switches, the switching mechanism will probably be FCP or FKE because of the CMOS integration constraint, although researchers from Lincoln Laboratory have shown that the thermo-optic effect (TO) in SOI can be sub-microsecond in its response and this would allow switching of “packets” in an on-chip network. The recent literature contains more examples of electrooptical switching in SiGe/Si structures than in SOI, but SOI switching will probably catch up soon. The work of Li et al.44,45 reveals a well-designed 3 x 2 free carrier injection switch in SiGe/Si waveguides, a device that also has wavelength multiplexing responses. Emelett and Soref46 have modeled a resonant, inplane 2 x 2 switch in SOI using two coupled microring resonators actuated, for example, by FCP. Lipson’s group at Cornell has shown experimentally47,48 that a PIN injector is quite effective in creating high concentrations of electrons and holes in an SOI microring resonator comprised of a circular deeply-etched ridge waveguide. Extending that result to multiple resonators, it appears that the PIN approach will be quite useful in making a ridge-type 2 x 2 dual-microring switch. MOS control is also available.49 I have not discussed optical control of switches and modulators, although this has been demonstrated and is useful in several situations.

6. PHOTODETECTORS

Among various 1.55 µm-photodiode contenders for CMOS-compatible integration on silicon OEICs, the germanium photodiode (typically under tensile strain) appears to be the winner. Several research groups have demonstrated the direct integration of Ge photodiodes upon silicon, and that process appears to have major importance for 1.55 µm applications. Several groups, among them MIT and Luxtera, have investigated this with promising results on responsivity and detectivity.

7. NANOSTRUCTURED PLASMON OPTICS

Plasmon optics is a new metallo-dielectric technology in which undoped silicon can serve as the “insulator” or “dielectric” in a composite photonic structure. Generally, photonic materials can be categorized by the sign of their dielectric constant ε and the sign of their permeability µ. A metal has (-ε, +µ) and is “singly negative,” whereas silicon
(+e, +u) is doubly positive. In the future, artificial or man-made materials with (-e, -u) and (+e, -u) will likely be synthesized. I believe that double and triple combinations of these four materials-types (composite photonic structures that include silicon, such as M-I-M or I-M-I) will prove to have unique and valuable optical properties.

Microphotonics refers to micrometer-scale devices. As to the wavelength scale, the minimum width of a silicon microphotonic strip waveguide (fundamental mode only) is approx \( \lambda/n \) where \( \lambda \) is the wavelength in vacuum and \( n \) is the core refractive index, while the interguide separation in a coupler is approx \( \lambda/2n \), the minimum feature size in microphotonics.

Photonic components with nanometer-scale features—“nanophotonics”—can be fabricated in several ways; for example, using quantum wires or quantum dots. A photonic crystal device is the prime example of nanophotonics and here the 2D dielectric lattice of holes or posts (or a 3D porous dielectric crystal) has a periodicity of order \( \lambda/n \) with a pore diameter \( \sim \lambda/n \). The PhC feature sizes are thus comparable to the microstrip sizes.

An idea of what can be accomplished with plasmon optics is given in the statement-of-work for a recent Multidisciplinary University Research Initiative (MURI) sponsored by the Air Force Office of Scientific Research (Dr. Gernot Pomrenke). This project, titled “Novel devices for plasmonic and nanophotonic networks” was launched in 2004 and will be carried out by scientists from Caltech, Stanford, Harvard, UCLA and UCSD. The goals and expected results of this multi-year program are well summarized on the website: www.plamonmuri.caltech.edu/research/index.html. Their objective is “to enable nanophotonic components for communications and imaging systems by exploiting localized and propagating surface plasmons that access nanometer-scale wavelengths at optical frequencies.” They say that “plasmon optics will open a new domain for integrated photonics based on: (1) extreme light localization—nonlinear excitations in ultrasmall volumes—compact, low-power optical devices, (2) very high spatial frequencies—an opportunity for optical imaging systems with nm-scale resolution, (3) enhanced light emission from active photonic devices via coupling to surface plasmons, (4) coupling from dielectric (fiber and SOI waveguide-based) photonics to plasmonic devices. The last point illustrates the new and promising linkage between microphotronics, PhC devices and plasmon-optic structures. On-chip, confined light can flow efficiently between a Si ridge, a plasmonic guide and PhC guide in any sequence. A fiber-accessible plasmon waveguide in a Si membrane has already been tested. Active plasmonic devices such as electrooptic waveguided modulators are at the frontier of research.

8. THE CONVERGENCE OF MICROPHOTONICS, NANOPHOTONICS, AND PLASMON OPTICS

I expect that the Si-based optical-network chip of the future will include integration of individual microphotonic, nanophotonic and plasmon-optic components along with “composite” components. In other words, a particular component may unite the micro, nano, plasmo techniques in some combination. A variety of interconnected photonic components comprising the network will be feasible This micro/nano/plasmo “convergence” is an emerging trend. As R&D proceeds, development of subwavelength plasmonics and refinements in nanodevices will drive the minimum feature size of photonic devices down towards the 10 nm quantum limit, thereby actualizing a “Moore’s Law for Photonics” which is discussed elsewhere in this conference by Dr. Jagdeep Shah and Dr. Mario Paniccia. Plasmonic devices can generally be “optically engineered” so that the minimum feature size is \( \lambda/10 \) or \( \lambda/20 \), which means that an active plasmonic device could have a length that is only one-tenth of the length required in active microphotonics.

8.1 Microphotonic Integration

There have been some notable examples. One is the “medium scale integration” in SOI obtained by a group in France\(^{31}\): an experimental 1.3 \( \mu \)m SOI ridge-waveguided low-loss 1 x 16 H-tree on-chip distributor using T-splitters, 90° mirrors, input grating and output gratings. This technique has potential for 1 x 256 optical clock distribution. Another example is the three dimensional integration of SOI strip waveguides with micro-disk photonic resonators via the 3D-sculpted-SIMOX technique\(^{32}\). This has potential for vertically coupled WDM filter banks.

8.2 Photonic-crystal component integration

Professor Dennis Prather’s group at the University of Delaware has made significant 2D planar integration of PhC components, for example, an etched SOI Si membrane containing J-couplers, line-defect waveguides, a negative-
refraction lens, a positive coupling lens, and a beamsplitter. His self-collimated dispersion-engineered PhC waveguides offer a major advance in guiding that eliminates line defects. A cone of light launched into the Si membrane travels in one, definite direction. This novel structure offers low propagation loss and allows several guided beams to intersect each other at right angles (in 2D or 3D) in a Manhattan grid topology that yields very low inter-guide crosstalk. Self-collimated channel waveguides, together with light deflecting elements, can be dispersion engineered within a 3D photonic crystal to enable photonic networks in 3D. All of the above are discussed at the University of Delaware website www.ece.udel.edu/~dprather/publications/publications091504.pdf. Of course, other research groups are active in PhC integration yielding PhC “circuits.” Various input/output coupling techniques are under study: for example, within a 3D photonic crystal, a hollow photonic-crystal horn antenna was integrated with a line-defect photonic-crystal channel waveguide, and the horn coupled free-space radiation into the guide.

Under its STTR program, AFOSR (Dr. Gernot Pomrenke) has sponsored research and technology transition that is relevant to Group IV photonics generally and to PhC integration specifically. By visiting the website www.dodsbir.net/selections/sttr1_04.htm#AF, one can find the Abstracts of the proposals selected for award on the silicon-related STTR topics: AF04-013, AF03-013, AF03-021, and AF02-017. Considerable innovation is shown here.

8.3 Hybrid integration of photonic-crystal structures with microstrip waveguides

Omega Optics and Prof. Ray Chen at UT-Austin have proposed (STTR AF04-13) to build an ultracompact modulator in silicon using a photonic-crystal-waveguide phase-modulator section hybrid-integrated in a microstrip Mach-Zehnder interferometer. The unique feature is that the MOS electrode length will be 100 times smaller than that in “conventional” microstrip because of the highly dispersive nature of the photonic crystal waveguide. Prof. Greg Nordin at UAH has built and tested several examples of hybrid integration; a rectangular “ring” resonator in microstrip guides with photonic-crystal 90° bends and PhC beamsplitting elements.

Concentration of the optical electric field is an important theme in silicon photonic components. The sub-λ high-index-contrast single mode SOI waveguides concentrate the field in a way useful for nonlinear optical effects. High-field resonators that are helpful in light emitters and IR switches have been studied, such as point-defect resonators in PhCs as well as microring- and microdisk-resonators. Compact geometries facilitate the E-concentration. Prof. Michal Lipson’s group reported a unique field concentrator consisting of Anderson localization in a 100 µm x 100 µm pseudo-random lattice of dielectric posts situated at the end of a microstrip waveguide.

SUMMARY

During the past four years, progress on Si-based photonic components has been impressive, and the thrust towards photonic integration on high-volume CMOS is proceeding rapidly with government sponsorship. Although development of electrically pumped 1.55 µm light sources is (temporarily?) lagging behind that of all the other 1.55 µm components (the integrated chip-scale microphotonic SOI waveguides, Ge photodiodes, ultrafast modulators, routing switches, couplers, splitters, gratings, tapers, isolators, and TE-TM polarizers) once thought to be exotic or marginal or impractical—these Si-based “circuit elements” will probably become “the” mainstream photonic devices. Throughout the wide infrared spectrum—NIR, MWIR, LWIR, far-IR and THz—opportunities and challenges exist for silicon-based PICs and OEICs. Photonic-crystal devices and the new plasmon-optic devices will contribute valuable functions to the Si PICs of the future, and the on-chip “convergence” of Si microphotronics, nanophotonics and plasmonics—an integration of techniques, is an emerging trend that results in ever-more-compact photonic devices—a miniaturization that may follow a “Moore’s Law for photonics.”

ACKNOWLEDGEMENT

The author wishes to thank AFOSR for sponsorship of his inhouse research at AFRL.

REFERENCES


